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| **TO BE COMPLETED BY STUDENT** | | |
| **INSTRUCTIONS: Shade (■) the appropriate boxes (**□) **where applicable, and delete the highlighted texts** | | |
| **Student Profiles** | | |
| **Registered as Group Number:** | | |
| **Assigned Final Demonstration Day:** □ Wednesday 14th November 2012 □ Friday 16th November 2012 | | |
| **Actual Final Demonstration Day:** □ Wednesday 14th November 2012 □ Friday 16th November 2012 | | |
| {**Delete this text** and paste your IVLE profile picture here for easy identification. If possible, do not resize the 120 x 160 image obtained from the IVLE profile. Automatic resizing of this table cell size is disabled and should not be manually changed. This space is reserved for the **photo of member 1**} | {**Delete this text** and paste your IVLE profile picture here for easy identification. If possible, do not resize the 120 x 160 image obtained from the IVLE profile. Automatic resizing of this table cell size is disabled and should not be manually changed. This space is reserved for the **photo of member 2**} | {**Delete this text** and paste your IVLE profile picture here for easy identification. If possible, do not resize the 120 x 160 image obtained from the IVLE profile. Automatic resizing of this table cell size is disabled and should not be manually changed. This space is reserved for the **photo of member 3**, if the group consists of 3 members} |
| {**Delete** this text and type the **name of member 1**} | {**Delete** this text and type the **name of member 2**} | {**Delete this text** and type the **name of member 3** if available} |
| {**Delete** this text and type the **student card ID of member 1**} | {**Delete** this text and type the **student card ID of member 2**} | {**Delete this** text and type the **student card ID of member 3** if available } |
| **COMMENTS BY EXAMINER** | | |
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| **TO BE COMPLETED BY STUDENT** | | |
| **Project Details** | | |
| **Name of Assembler / Compiler Used:** □ Keil C51 □ Others (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_) | | |
| **Number of .bit files used during demonstration:** □ 1 □ 2 □ More than 2 | | |
| **Number of working instructions present in VHDL code:** | | |
| **Total number of instructions used in final demonstration program:** | | |
| **Number of unique instructions used in final demonstration program:** | | |
| **Usage of components connected to the FPGA:**  □ Yes □ No | | |
| **External components used:**  *(For this module, students should take note that the focus is to demonstrate the capabilities of the computer architecture, and NOT on the complexity of the hardware used)* | □ Keypad □ LCD □ PC  □ TTL Chips (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_)  □ Others (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_) | |
| **Brief description of final demonstration:**  *(Ideally, the description should be around 10 to 20 words, with a maximum of 50 words. More details can be presented in the report)* | {**Delete this text**. For record purposes, paste a picture of your connected final demonstration hardware if available. Automatic resizing of this table cell size is disabled and should not be manually changed. If a photo is not available, still delete this text} | |
| **Declaration of Implementation (Tested and Working) By Student** | | |
| **Interrupts:** □ External 0 □ Timer 0 □ External 1 □ Timer 1 □ Serial Port | | |
| **Interrupt Priority Level Structure:** □ High-priority and low-priority □ Priority within Level | | |
| **Timer 0 and Timer 1:** □ Mode 0 □ Mode 1 □ Mode 2 □ Mode 3 | | |
| **Serial Port:** □ Mode 0 □ Mode 1 □ Mode 2 □ Mode 3 | | |
| **External memory:** □Simulated and working perfectly □ Shown through FPGA demonstration | | |
| **Optimisations:** □ Not available □ Available, with detailed description in report | | |
| **Brief description of optimisation if available**: | | |
| **Brief mention of details that students would like to make known to the examiner to differentiate their program from others**: *(Examples include complex instructions, communication between two FPGAs, etc... The detailed description should be present in the report)* | | |
| **We declare that the information provided by the team is correct and that we will be able to answer questions regarding these instructions and implementations during the final demonstration. We confirm that the working VHDL codes for these implementations and instructions will be uploaded to IVLE by the deadline stated in the document “CG3207 Final Instructions”.** | | **Signature of Members:** |
| **FOR USE BY TA** | | |
| **Assessed as:** □ Group □ Sub-group (Members: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_) | | |
| **Section A** | | |
| **□□ representing: Demonstrated through FPGA or others, Verified VHDL code presence** | | |
| **Interrupts:** □□ External 0 □□ Timer 0 □□ External 1 □□ Timer 1 □□ Serial Port | | |
| **Interrupt Priority Level Structure:** □□ High-priority and low-priority □□ Priority within Level | | |
| **Timer 0 and Timer 1:** □□ Mode 0 □□ Mode 1 □□ Mode 2 □□ Mode 3 | | |
| **Serial Port:** □□ Mode 0 □□ Mode 1 □□ Mode 2 □□ Mode 3 | | |
| **External memory:** □□ | | |
| **Optimisations:** □□ | | |
| **Architecture Timing Comments:** | | |
| **Section B** | | |
| **Deadline met:**  □ Final demonstration on scheduled day □ Report during demo. □ Softcopy items on IVLE | | |
| **Report:**  [ ] Report presentation grade [ ] Contents quality grade | | |
| **Proof of Understanding:** □ During final demonstration □ Through report □ Others | | |
| **Academic Integrity Comments:** | | |